CORRECTED VERSION* PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : G06F 12/00 — A1

(11) International Publication Number: WO 90/04830

(43) International Publication Date: 3 May 1990 (03.05.90)

(21) International Application Number: PCT/US89/04668

(22) International Filing Date: 18 October 1989 (18.10.89)

(30) Priority data:
260,256 — 20 October 1988 (20.10.88) — US
353,179 — 3 May 1989 (03.05.89) — US

(71) Applicant: UNIVERSITIES SPACE RESEARCH ASSOCIATION [US/US]; The American City Bldg., Suite 212, Columbia, MD 21044 (US).

(72) Inventor: JAECKEL, Louis, A. ; 756 Oak Street, E, Ukiah, CA 95482 (US).

(74) Agent: SMITH, Joseph, H.; 4410 Casa Madeira Lane, San Jose, CA 95127 (US).

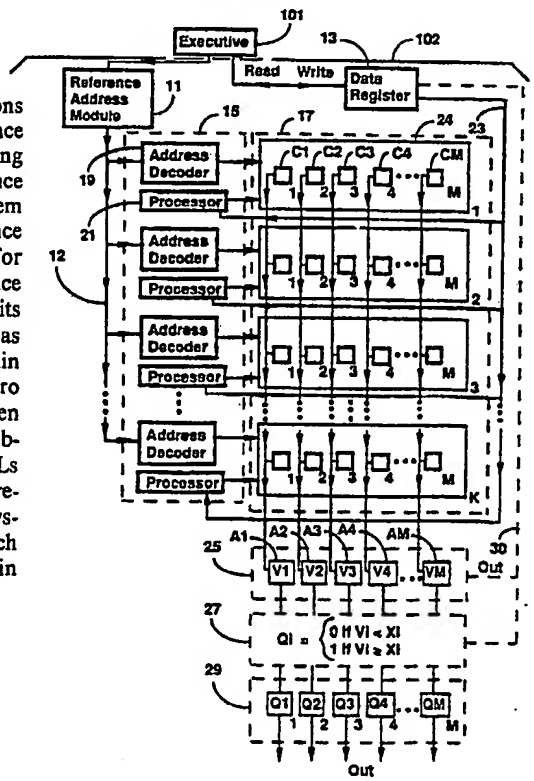
(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB, GB (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.

(54) Title: METHOD AND APPARATUS FOR A SPARSE DISTRIBUTED MEMORY SYSTEM

(57) Abstract

A computer memory system (102) includes k hard memory locations (HMLs) (24), each HML (24) comprising M counters (C1-CM). A reference address element (11) stores a reference address, the reference address being a sequence of N bits. A data register element (13) stores data as a sequence of M integers. In addition, the memory system (102) has a processor system (15) for determining a subset of HMLs (24) to activate for each reference address and for activating those HMLs (24) during reads and writes. For each HML (24), the processor system (15) receives a subset of the reference address bits equal in number to q. The subset of the reference address bits is chosen by selecting, for each HML (24), q integers between 1 and N as selected coordinates (SCs), each SC corresponding to a bit position within the reference address, and for each SC for each HML (24), assigning a zero or one as an assigned value for that SC. The processor system (15) then stores the SCs and the assigned values and in response to receiving the subset of the reference address bits, for each of the SCs for each of the HMLs (24), compares the assigned value for the SC with the value of the corresponding bit in the subset of the reference address bits. The processor system (15) then provides an activation signal for those HMLs (24) for which the assigned values for all SCs are identical with the corresponding bits in the subset of the reference address bits.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria
AU	Australia
BB	Barbados
BE	Belgium
BF	Burkina Faso
BG	Bulgaria
BJ	Benin
BR	Brazil
CA	Canada
CF	Central African Republic
CG	Congo
CH	Switzerland
CM	Cameroon
DE	Germany, Federal Republic of
DK	Denmark
ES	Spain
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
HU	Hungary
IT	Italy
JP	Japan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
LI	Liechtenstein
LK	Sri Lanka
LU	Luxembourg
MC	Monaco
MG	Madagascar
ML	Mali
MR	Mauritania
MW	Malawi
NL	Netherlands
NO	Norway
RO	Romania
SD	Sudan
SE	Sweden
SN	Senegal
SU	Soviet Union
TD	Chad
TG	Togo
US	United States of America